A1 (cont'd)

each of capacitors CC and CD and (b) either the variable capacitance of varactor CE or twice the variable capacitance of varactor CF. A control voltage (not shown) is applied to varactor CE or CF to control its AC capacitance and thus frequency f_O.

A2

[0022] Wong et al ("Wong"), "A Wide Tuning Range Gated Varactor," IEEE J. Solid-State Circs., May 2000, pages 773 - 779, describes another type of semiconductor varactor. As generally shown in Fig. 7, Wong's varactor is created from n body region 60 of a semiconductor body. Using somewhat unusual terminology, Wong's varactor includes heavily doped p-type "source" 62 and heavily doped n-type "drain" 64 laterally separated from each other along the upper semiconductor surface. Gate dielectric layer 66 separates gate electrode 68 from moderately doped n-type body material situated between source 62 and drain 64. Wong reports that the varactor capacitance is defined as the capacitance looking into the drain node.

A3

[0027] The present invention furnishes a semiconductor junction varactor that employs gate enhancement for enabling the varactor to achieve a high ratio of maximum varactor capacitance to minimum varactor capacitance. The maximum-to-minimum capacitance ratio for the present gate-enhanced junction varactor can easily be well in excess of 10. More particularly, the present varactor can readily achieve a maximum-to-minimum capacitance ratio in the vicinity of 20 or more. The varactor of the invention is of relatively simple design. No special processing techniques are needed to fabricate the present varactor. Consequently, it can be fabricated according to a semiconductor manufacturing process having a capability for providing p-n diodes and insulated-gate FETs.

A4

[0072] With body voltage V_B applied to body electrode 116, gate-to-body bias voltage V_{GB} is applied between gate electrode 112 and body electrode 116 by applying a DC gate voltage V_G to gate electrode 112. Gate-to-body voltage V_{GB} is specifically defined as:

$$V_{GB} = V_G - V_B \qquad (11)$$

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where gate voltage V_G is defined relative to the same arbitrary reference point, e.g., ground, as plate voltage V_P and body voltage V_B. Gate-to-body voltage V_{GB} is generally at least zero and is normally positive. As discussed further below, voltage V_{GB} is normally substantially constant or is controlled as a function of plate-to-body voltage V_R.

[0096] Thickness values t_{dJmax} and t_{dJmin} for junction depletion region 118 can be determined approximately from Eq. 3 presented above for the conventional junction varactor of Fig. 3. For uniform acceptor body dopant concentration N_B in region 118, the maximum-to-minimum thickness ratio for region 118 is approximately:

$$\frac{t_{dJmax}}{t_{dJmin}} = \sqrt{\frac{V_{Rmax} + V_{BI}}{V_{Rmin} + V_{BI}}} \qquad (23)$$

where V_{BI} is the built-in voltage of p-n junction 104. The right-hand side of Eq. 23 is the maximum-to-minimum varactor capacitance ratio given by Eq. 4 for the conventional junction varactor of Fig. 3 at uniform body dopant concentration in body-side portion 32 of junction depletion region 30. If gate electrode 110 were absent so that inversion area A_I is zero in the varactor of Fig. 8, the capacitance ratio given by Eq. 22 for the present gate-enhanced junction varactor would (as expected) devolve to that given by Eq. 4 for the conventional junction varactor.

[0097] In addition to the t_{dJmax}/t_{dJmin} junction depletion thickness ratio, the maximum-to-minimum varactor capacitance ratio for the varactor of Fig. 8 contains, as indicated by Eq. 22, a factor $(A_I/A_P)(t_{dJmax}/t_{dsmin})$ that arises from the gate enhancement. The t_{dJmax}/t_{dsmin} mixed gate-enhancement thickness ratio is greater than 1. Accordingly, the maximum-to-minimum varactor capacitance ratio for the varactor of Fig. 8 can be made quite high by choosing the A_I/A_P gate-enhancement area ratio to be high.

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[0107] In addition, the p-channel junction varactor of Fig. 10 contains a gate dielectric layer 160, a gate electrode 162, a plate electrode 164, a body electrode 166, a junction depletion region 168 consisting of a body-side portion 170 and a plate-side portion 172,

undepleted p-type material 174 of plate region 152, a surface depletion region 176, and undepleted n-type material 178 of body region 150. An inversion layer 180, here consisting of holes, is formed along upper semiconductor surface 156 below gate dielectric layer 160 and gate electrode 162 to meet plate region 152. Voltages V_G, V_P, and V_B are respectively applied to electrodes 162, 164, and 166 in the p-channel varactor of Fig. 10 to establish gate-to-body voltage V_{GB} and plate-to-body voltage V_R according to Eqs. 10 and 11 just as voltages V_G, V_P, and V_B are applied to electrodes 112, 114, and 116 in the n-channel varactor of Fig. 8.

[0112] Assume that acceptor dopant concentration N_B in the body material that forms surface depletion region 126 and body-side portion 120 of junction depletion region 118 in the varactor of Fig. 8 is uniform. For simplicity, also assume that body voltage V_B is ground reference (0 V). The V_X derivation can then be done in terms of plate-to-body voltage V_R and gate-to-body voltage V_{GB} without reference to plate voltage V_P and gate voltage V_G since they respectively equal voltages V_R and V_{GB} when body voltage V_B is ground.

[0114] Let V_{IL} generally represent the DC electrical potential of inversion layer 130 in Fig. 8. Neglecting the vertical potential drop in layer 130, inversion-layer potential V_{IL} is at an initial DC value V_{ILi} given as follows when plate-to-body voltage V_R is zero and the varactor of Fig. 8 is in strong inversion:

$$\begin{aligned} V_{ILi} &= \Phi_{s,inv} \\ &= 2\Phi_{Fp} \end{aligned} \tag{24}$$

where $\Phi_{s,inv}$ is the surface potential at inversion, and Φ_{Fp} is the Fermi potential of the p-type semiconductor material in surface depletion region 126. Fermi potential Φ_{Fp} is determined from:

$$\Phi_{Fp} = \left(\frac{kT}{q}\right)\ln\left(\frac{N_B}{n_i}\right) \tag{25}$$

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A8 (cont'd)

where k is Boltzmann's constant, T is the temperature, and n_i is the intrinsic carrier concentration.

[0116] Gate dielectric layer 112 takes up the potential between body region 100 and inversion layer 130. The DC potential difference V_{GD} across gate dielectric 112 is at an initial DC value V_{GDi} given as:

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$$\begin{aligned} V_{GDi} &= V_{GB} - V_{FB} - V_{ILi} \\ &\approx V_{GB} - V_{FB} - 2\Phi_{Fp} \end{aligned} \qquad (27)$$

where V_{FB} is the flat-band voltage.

[0150] High-bias impedance component ZH is part of a high-bias electrically conductive DC path which extends through circuit 230 and through which high-bias capacitance signal path line 236 is electrically coupled to the V_{HH} high voltage supply. Low-bias impedance component ZL is similarly part of a low-bias electrically conductive DC path which extends through circuit 230 and through which low-bias capacitance signal path line 238 is electrically coupled to the V_{LL} low voltage supply.

A10

[0168] The general circuitry of Fig. 17 can be readily modified to use a p-channel version of the present gate-enhanced junction varactor in place of n-channel junction varactor C1. One way of implementing this modification is to reconfigure the circuitry so that it is interconnected in a complementary (mirror-image) manner to what is shown in Fig. 17. That is, high-bias capacitance signal path line 236 can be connected directly to voltage sources 244 and 246 in control system 232. Using the electrode reference symbols of Fig. 10, low-bias capacitance signal path line 238 is connected to plate electrode 164 of the p-channel varactor. With the polarity direction of voltage sources 244 and 246 reversed, gate electrode 162 and body electrode 166 of the p-channel varactor are respectively connected to voltage sources 244 and 246. Due to the polarity direction reversal, voltage source 244 provides gate voltage

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A11 (cont'd)

V_G at a lower value than body voltage V_B provided by voltage source 246. When present, level shifter 234 is connected between circuit 230 and the V_{LL} supply.

A12

[0175] Varactor control system 232 in the circuitry of Fig. 18 is configured with respect to, and controls, varactor C1 in the same manner as in the circuitry of Fig. 17. Control system 232 in the circuitry of Fig. 18 is also configured with respect to, and controls, varactor C2 the same as varactor C1. Hence, system 232 furnishes each of varactors C1 and C2 with gate voltage V_G and body voltage V_B at values which normally vary during circuitry operation but whose difference V_{GB} is held largely constant at initial value V_{GBi}. In particular, high-bias DC voltage source 244 provides gate voltage V_G on high-bias control line 240 to gate electrode 112 of each of varactors C1 and C2. Low-bias voltage source 246 provides body voltage V_B on low-bias control line 242 to body electrode 116 of each of varactors C1 and C2.

A13

[0180] Subject to the above-mentioned configurational differences, the circuitry of Fig. 18 operates similarly to, but in a symmetrical manner compared to, the circuitry of Fig. 17. Plate voltages V_P and V_{PF}, the DC portions of respective composite plate voltages v_P and v_{PF} provided from circuit 260 to plate electrodes 114 of varactors C1 and C2 are maintained largely constant. Each DC plate voltage V_P or V_{PF} exceeds body voltage V_B. Due to the circuitry symmetry, plate voltages V_P and V_{PF} are largely equal.

A14

[0203] Fig. 20a illustrates how widthwise lineal capacitance C_{VW} varies with plate-to-body voltage V_R for the simulated varactor of Fig. 15 when gate-to-body voltage is adjusted according to the condition of Eq. 45 with gate-to-plate voltage V_{GP} being set at zero-point gate threshold value V_{T0}, approximately 0.45 V. See curve 266 defined by circles in Fig. 20a. For reference purposes, Fig. 20a also repeats the six curves of Fig. 16 at constant values of voltage V_{GB}. As curve 266 indicates, adjusting voltage V_{GB} so that voltage V_{GP} is held constant at threshold value V_{T0} enables capacitance C_{VW} to decrease gradually with increasing voltage V_R and thereby avoids the sharp C_{VW} change that occur when voltage V_{GB} is constant. This significantly facilitates controlling the varactor capacitance and alleviates problems caused by noise in the control path.

[0204] Fig. 20b depicts how lineal capacitance C_{VW} varies with plate-to-body voltage V_R for the present simulated varactor when gate-to-body voltage V_{GB} is controlled according to Eq. 45 with gate-to-plate voltage V_{GB} fixed at values ranging from 0.3 V in 0.1-V increments

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to 0.6 V. See curves 268A, 268B, 268C, and 268D defined by circles in Fig. 20b. As in Fig. 20a, the six curves of Fig. 16 at constant values of voltage V_{GB} are also repeated in Fig. 20b for reference purposes.

[0205] Curves 268A, 268B, 268C, and 268D in Fig. 20b show that the C_{VW} variations with plate-to-body voltage V_R becomes progressively more gradual as gate-to-plate voltage V_{GP} is raised from a constant value of 0.3 V to a constant value of 0.6 V. Also, capacitance C_{VW} for each of curves 268A, 268B, 268C, and 268D changes approximately linearly with increasing voltage V_R over the majority of the minimum-to-maximum varactor capacitance range. This further simplifies controlling the varactor capacitance as a function of voltage V_R.

A14

[0206] Among the four values of gate-to-plate voltage V_{GB} presented in Fig. 20b, fixing voltage V_{GP} at 0.6 V as represented by curve 268D generally enables the varactor capacitance to be controlled best because the change in varactor capacitance with increasing plate-to-body voltage V_R is most gradual. Other considerations may place the optimum value of voltage V_{GB} at a point between 0.5 V and 0.6 V.

[0216] A composite gate voltage v_G consisting of DC gate voltage V_G and an AC gate voltage v_g is provided from electronic circuit 270 on electrical line 276 to gate electrode 112 of varactor C1. Impedance component ZU is of such a nature in some implementations of circuit 270 that substantially no DC voltage drop occurs across component ZU. Since the ZU DC path connects line 276 to the V_{HH} high voltage supply, DC gate voltage V_G is then simply high voltage supply V_{HH}, normally substantially constant. In further implementations where component ZU is of substantially zero impedance, AC gate voltage v_g is substantially zero. Composite gate voltage v_G then devolves to DC gate voltage V_G which equals V_{HH}.

A15

[0219] In some implementations of circuit 270, impedance components ZH, ZT, and ZU are of such a nature that DC impedance voltage drop V_Z is very close to zero. Gate-to-plate bias voltage V_{GP} then approximately equals DC setter voltage V_{VS}. Regardless of whether impedance voltage V_Z is zero or some positive constant value, voltage setter 274 controls the value of voltage V_{GP}. Importantly, voltage V_{GP} is controlled by the circuitry of Fig. 21 so as to be largely constant during circuitry operation.

A16

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[0222] In addition to often being largely constant at high supply voltage V_{HH} or at a value close to V_{HH}, DC gate voltage V_G is normally greater than DC body voltage V_B. Adjusting

A17

body voltage V_B upward or downward produces an opposite change in gate-to-body voltage V_{GB} which, in turn, produces an opposite change in plate-to-body voltage V_R while gate-to-plate voltage V_{GP} is being held largely constant at $V_{VS} + V_Z$, often approximately V_{VS}. Varactor C1 again operates internally as described above in connection with the varactor of Fig. 8. Varactor capacitance C_V is thereby adjusted in the way generally described above in connection with Eq. 45 to enable the circuitry of Fig. 21 to perform an electronic function that varies with the C_V value.

[0230] Analogous to impedance component ZU in the circuitry of Fig. 21, impedance component Z3 is part of an electrically conductive DC path which extends through circuit 280 and through which electrical line 276 connected to C1 gate electrode 112 is electrically coupled to the V_{HH} high voltage supply. Impedance component Z4 is similarly part of an electrically conductive DC path which extends through circuit 280 and through which an electrical line 282 connected to C2 gate electrode 112 is electrically coupled to the V_{HH} supply. Analogous to impedance component ZH in the circuitry of Fig. 21, impedance component Z5 is part of a electrically conductive DC path which extends through circuit 280 and through which voltage setter 274 is electrically coupled to the V_{HH} supply. Accordingly, impedance components Z3, Z4, and Z5 are parts of a pair of longer electrically conductive DC paths through which paths 236 and 262 are electrically coupled to the V_{HH} supply.

[0234] Similar to the circuitry of Fig. 18, the second ends of the C1 and C2 capacitance signal paths terminate at the V_{LL} low voltage supply in the circuitry of Fig. 22. The C1 capacitance signal path in Fig. 22 specifically consists of high-bias capacitance signal path line 236, C1 plate electrode 114, C1 body electrode 116, control line 242, voltage source 278, and electrical line 284. The C2 capacitance signal path similarly consists of high-bias capacitance signal path line 262, C2 plate electrode 114, C2 body electrode 116, line 242, voltage source 278, and line 284. Gate electrodes 112 of varactors C1 and C2 are again outside the capacitance signal paths.

[0242] Voltage setter 274 is implemented as a p-n diode D2 which couples the V_{HH} supply to the upper ends of inductors L1 and L2. Setter voltage drop V_{VS} here is a diode forward voltage drop V_F of 0.5 - 0.9 V, again typically 0.7 V. Diode D2 and current source I1 cooperate to set the specific value of diode drop V_F. As with diode D1 and current source I1 in the VCO of Fig. 19, increasing the size of current source I1 so as to increase its current

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causes voltage V_F to increase, and vice versa. Since impedance voltage V_Z is largely zero, each of DC gate-to-plate bias voltage V_{GP} and V_{GPF} is largely setter voltage drop V_{VS} and thus equals V_F. Each of DC plate voltages V_P and V_{PF} is largely fixed at $V_{HH} - V_F$.

A20 (cont'd)

[0257] A layer 290 of dielectric material overlies field insulating region 134 and semiconductor islands 136 and 138 above gate electrode 112 in the varactor of Figs. 24 and 25. Plate electrode 114 contacts plate region 102 through a plate contact opening 292 extending through dielectric layer 290. Body electrode 116 contacts body contact portion 132 of body region 100 through a group, fourteen in the exemplary layout of Fig. 24, of body contact openings 294 extending through layer 290. Body contact openings 294 are distributed relatively uniformly across the lateral area occupied by body contact portion 132 to provide uniform electrical connection to body region 100. A gate contact opening 296 extends through layer 290. An electrical conductive gate line 298, typically consisting of the same metallic material as plate electrode 114 and body electrode 116, contacts gate electrode 112 through gate contact opening 296.--

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Enclosed are copies of specification pages 2, 8 - 10, 17, 25, 26, 28 - 31, 43, 47, 49, 50, 56, 57, 59 - 61, 63, 64, 66, and 70 in which the changes to the foregoing paragraphs are indicated in red.

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